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Proton Single Event Effects Radiation Test Report

for the

RHrFPGA Radiation-Hardened Field-Programmable Gate Array

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1	Add “Proton” to cover page title. Correct last entry in Table 3.3-I. Clarify terminology in last two paragraphs of section 5.2.	2004-01-09 jl/JL

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1.0 INTRODUCTION

This report describes a proton single event effects (SEE) test of three RHrFPGA integrated circuits (IC). Goddard Space Flight Center (GSFC) personnel performed the test at the Indiana University Cyclotron Facility (IUCF) on 30 October 2003 with assistance from Honeywell's RHrFPGA design and test team.

The test characterized RHrFPGA sensitivity to proton-induced single event upset (SEU). The test procedure included six different test programs and FPGA configurations, which were optimized to evaluate the RHrFPGA's two unique types of internal memory elements and to exercise the device in a mode representative of a current RHrFPGA application. The bistable storage elements within the RHrFPGA are the chip's internal configuration RAM (131152 bits), 6400 application flip-flops, and additional control flip-flops. All were designed to be SEU-hard and were not expected to be vulnerable to proton-induced SEU.

Each RHrFPGA test device was irradiated to a proton fluence of 3.4 $x10^{13}$ p/cm^2 at 203 MeV beam energy, corresponding to 2.0 Mrad(Si) total dose per device. The test parts did not exhibit SEU or any other SEE, demonstrating that the RHrFPGA is essentially immune to proton-induced SEU.

Although the RHrFPGA devices did not upset during the proton test, the test results can still be used to establish upper limits for device proton SEU rates. This is accomplished by assuming the occurrence of 1 upset in each type of memory cell at the tested proton fluences. In this case the resulting SER calculations serve as an indicator of test rigor and do not imply an actual sensitivity to proton-induced SEU. Table 1-1 presents the limiting SER predictions for multiple trapped and galactic proton environments. Two sets of assumptions were used in the calculations: Nominal Upper Bound, and Extreme Worst Case. These are described in more detail in section 5.

Table 1-I RHrFPGA Test Results - Limiting Proton SEU Rates.

Orbit	Environment	Worst-Case Soft Error Rates (Upsets/bit/day) (1)			
		Nominal Upper Bound SER		Extreme Worst-Case SER	
		RAM Cell	Flip-Flop	RAM Cell	Flip-Flop
2058 x 2058 km x 63°	AP8MIN (2)	$< 1.1x10^{-11}$	$< 4.3x10^{-10}$	$< 3.3x10^{-11}$	$< 1.5x10^{-09}$
1470 x 1470 km x 53°	AP8MIN	$< 4.7x10^{-12}$	$< 1.8x10^{-10}$	$< 1.4x10^{-11}$	$< 6.2x10^{-10}$
926 x 926 km x 57°	AP8MIN	$< 7.3x10^{-13}$	$< 2.8x10^{-11}$	$< 2.3x10^{-12}$	$< 1.0x10^{-10}$
800 x 800 km x 98°	AP8MIN	$< 3.6x10^{-13}$	$< 1.4x10^{-11}$	$< 1.0x10^{-12}$	$< 4.7x10^{-11}$
450 x 450 km x 51.6°	AP8MIN	$< 2.3x10^{-15}$	$< 8.9x10^{-14}$	$< 5.8x10^{-15}$	$< 2.6x10^{-13}$
35796 x 35976 km x 0°	CREME96 [3], solar minimum	$< 1.7x10^{-14}$	$< 6.5x10^{-13}$	$< 4.3x10^{-14}$	$< 1.9x10^{-12}$

(1) – SER in specified orbit and proton radiation environment, 100 to 150 mils Al shielding
(2) – AP8 trapped proton environment [1] at solar minimum
(3) – CREME96 [2] solar minimum galactic cosmic ray environment, no geomagnetic shielding

2.0 DEVICE DESCRIPTION

The RHrFPGA is an SRAM-based (soft configurable) field-programmable gate array manufactured by Honeywell using a radiation-hardened silicon on insulator fabrication process. It has 6400 user-configurable logic cells and 131152 configuration SRAM cells. NASA GSFC funded the development, fabrication, and radiation testing of the RHrFPGA.

3.0 TEST DESCRIPTION

The RHrFPGA heavy ion SEE test was performed at the Indiana University Cyclotron Facility's Radiation Effects Research Program 1 (RERP1) facility. Steve Buchner, Hak Kim, and Tony Sanders of GSFC managed the test and provided some essential test equipment. Craig Ross, Bill Burns, and John Lintz of Honeywell planned the test and operated the characterization test set. Barbara Von Przewoski and Tony Kinser of IUCF operated the proton beam and provided radiation dosimetry services.

3.1 Test Facility and Radiation Source

IUCF personnel delivered a 203 MeV proton beam to the RHrFPGA test devices in the RERP-1 target room. The beam profile was established using a thin beam spreader, which maximizes intensity and yields 70% uniformity over a 1" diameter beam spot. A 1" square collimator was placed on the beam exit pipe to minimize the area of the test fixture outside of the RHrFPGA device that would be irradiated. Test fluences up to 2.0×10^{10} p/cm^2 were attained in the test.

3.2 Test Configuration

Test personnel configured the radiation test assembly per Figure 3.2-1. An RHrFPGA test card containing two RHrFPGA devices was placed in the path of the proton beam. One RHrFPGA device functioned as a test device, and a second RHrFPGA device functioned as a test controller to sequence the test and detect upsets in the test device. The controller FPGA also maintained test health status and SEU error counts of the test device in a set of registers. The test controller repeatedly output the test status words to an oscilloscope that was monitored by test personnel.

The RHrFPGA memory elements uses SEU hardening techniques similar to, but more aggressive than, those of Honeywell's HX6408 SRAM. The HX6408 SRAM proton SEU cross-section was shown to be very sensitive to the proton angle of incidence on the die, with grazing angles yielding the highest cross-sections [3]. This sensitivity was attributed a single secondary heavy ion hitting two transistors within a memory cell [4, 5]. Based on this model, the SEU cross-section is highest for a proton angle of incidence parallel to the path between the two sensitive transistors in a cell. A grazing (parallel) proton beam oriented normal to this path is thus expected to produce an SEU cross-section similar to a normal incidence beam. For these reasons, Honeywell designed the test to irradiate the RHrFPGA devices with the proton beam nearly parallel to the die surface and with the die oriented so that the beam parallels the sensitive path

direction. However, the optimum orientations for the configuration RAM and application flip-flop are orthogonal to each other, so this necessitated different orientations for testing the two cell types as noted in Figure 3.2-1. Also, the rotation angle was limited to 70° from normal for this test due to alignment difficulties and concerns of irradiating the controller device at steeper angles. As a result, all exposures were performed at a 70° angle of incidence, using different axes of rotation for the two cell types. Figure 3.2-2 illustrates the fixture configuration and memory cell orientations within the die.

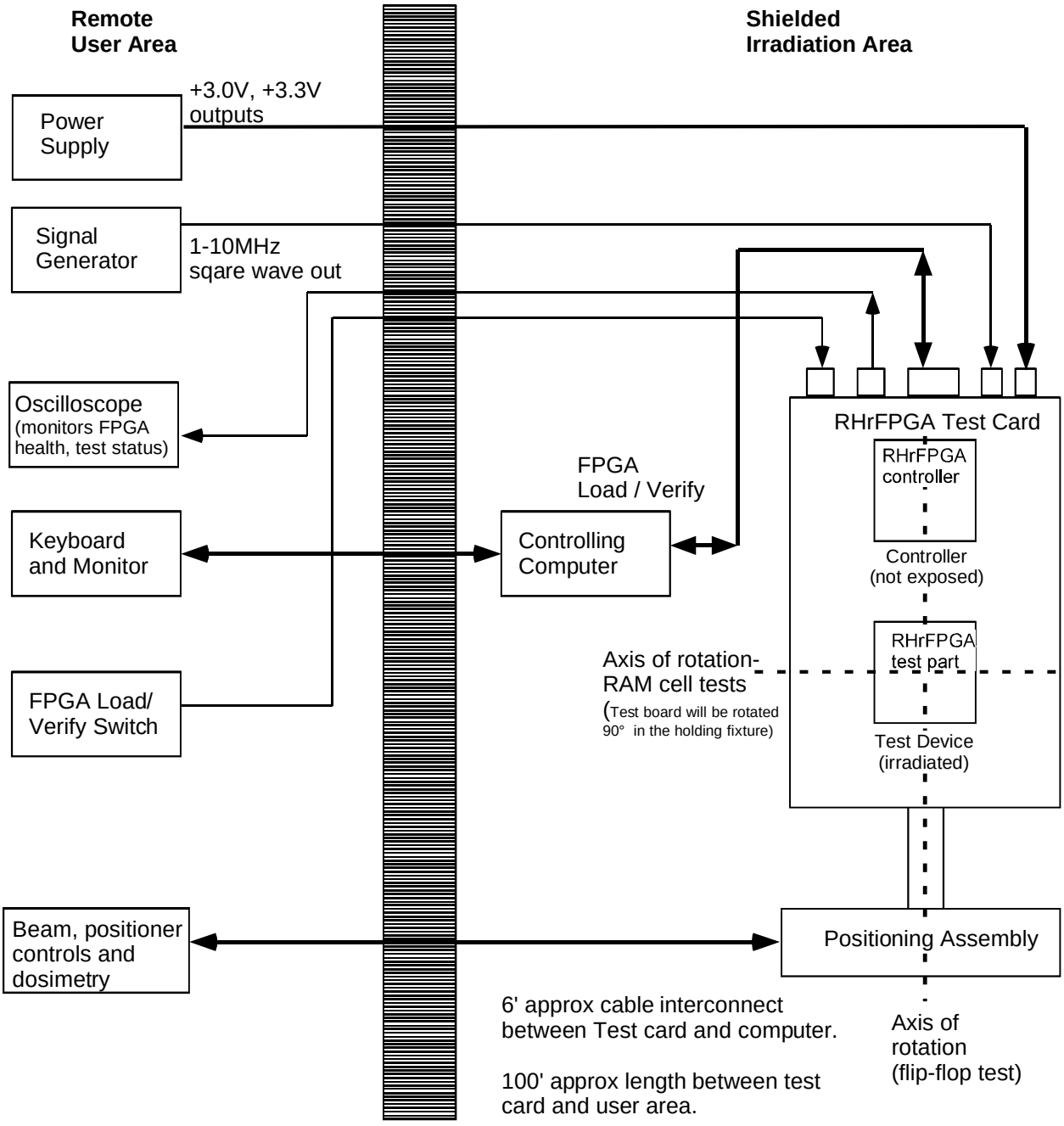
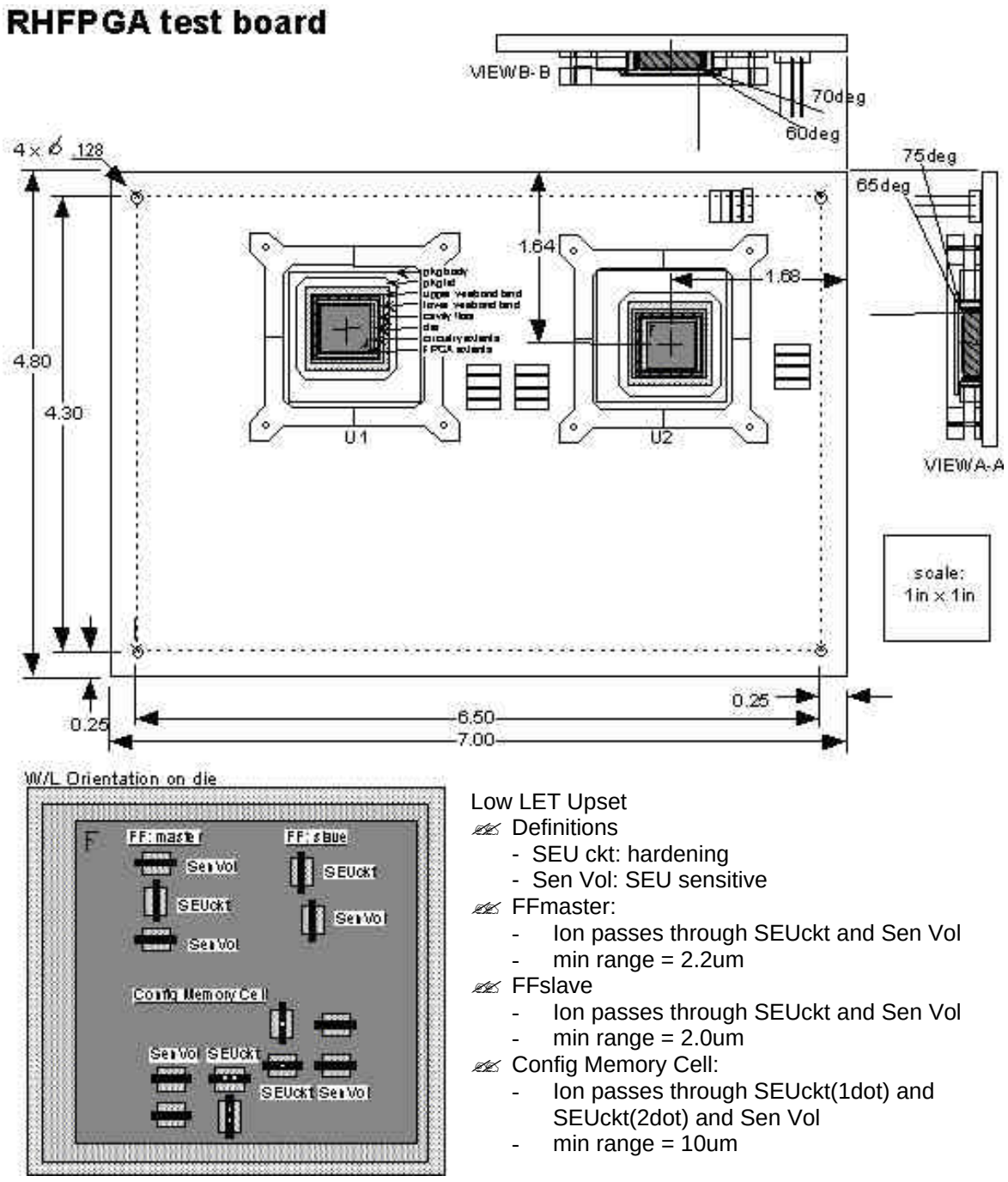


Figure 3.2-1 RHrFPGA Proton SEU Test Assembly Configuration.



Low LET Upset

- Definitions
  - SEU ckt: hardening
  - Sen Vol: SEU sensitive
- FFmaster:
  - Ion passes through SEUckt and Sen Vol
  - min range = 2.2um
- FFslave
  - Ion passes through SEUckt and Sen Vol
  - min range = 2.0um
- Config Memory Cell:
  - Ion passes through SEUckt(1dot) and SEUckt(2dot) and Sen Vol
  - min range = 10um

Figure 3.2-2 RHrFPGA Proton SEU Test Fixture and Die Layout.

3.3 Test Programs (Vectors)

Table 3.3-I lists the six RHrFPGA SEU characterization test programs. The "Application" test is an actual RHrFPGA application that implements a demodulator algorithm. The "Shift Register" tests continuously exercise serial chains of shift

registers. Variations of this test include specific combinatorial logic elements and interconnect logic within the chip as indicated in each test name. The “5760” test characterizes a large number of flip-flops. It was performed with the chip in the worst-case available die orientation to cause upset of the flip-flop cell, while the other tests were performed in the worst-case available die orientation for upset of the RAM cell.

Table 3.3-I RHrFPGA Test Programs (Vectors).

Test #	Fixture Orientation (1)	Test Program Name	Abbreviated Name	Flip-Flops Tested	Configuration RAM Bits Tested
1	RAM	Application with I/O (Demodulator)	Application	1506	131152
3.2	RAM	Full Shift Register Vertical	SR-Vert	1450	131152
3.6	RAM	Shift Register with Lbus	SR-Lbus	670	131152
3.4	RAM	Shift Register with Logic	SR-Logic	297	131152
3.5	RAM	Shift Register with Xbus	SR-Xbus	184	131152
3.8	Flip-Flop	5760	5760	5790	131152

(1) – Identifies the cell type that was placed in the worst-case orientation to produce SEU. The orientations for the two cell types are orthogonal to each other.

3.4 Test Procedure

Seventeen exposure runs were done to test the RHrFPGA for SEU and SET at the minimum specified supply voltage of 3.0V and room temperature. Two parts were exposed in the worst-case orientation for configuration RAM upset, and one was exposed in the worst-case orientation for flip-flop upset. Test personnel followed these steps in the conduct of each exposure run. The test device’s configuration SRAM was checked for upset at the conclusion of each test run.

1. Establish the correct test conditions (proton energy, fixture position, incidence angle, supply voltage, maximum fluence setting).
2. Load the RHrFPGA controller and test device with the proper configurations to support the test. Verify that the test device and test set are functioning correctly.
3. Irradiate the test device to the desired test fluence while monitoring the device for SEU and monitoring the test set for proper health.
4. Read the controller status registers to determine the number of upsets or test anomalies that occurred in the test.
5. Read the test device configuration to check for configuration SRAM upsets.
6. Record all relevant test data from the exposure run.
7. Return to step 1 for the next exposure run until the test is finished.

4.0 TEST RESULTS

The three RHrFPGA devices did not experience SEU or other SEE at a proton fluence of 3.4x10^{13} p/cm^2 per test device. This result was consistent with analytical predictions indicating the device is not sensitive to proton induced SEE. All parts survived 2.0 Mrad(Si) total dose with no observed degradation. Table 4-I presents the SEU test log.

4.1 Limiting SEU Cross-Sections

Test runs 1-13 evaluated the RHrFPGA in the optimized orientation for configuration RAM upset. Two devices each received 3.4 x10^{13} p/cm^2 fluence with zero upsets. Neglecting the fluence accumulated during the remaining test runs, the limiting SEU cross-section is calculated as follows.

1 ? (3.4 x10^{13} p/cm2/device x 2 devices x 131152 bits/dev) = 1.12x10^{-19} cm^2/bit (1)

Test runs 14-17 evaluated one RHrFPGA in the optimized orientation for Flip-Flop upset. Neglecting fluence accumulated in the other test orientation, the limiting SEU cross-section from the test is calculated as follows.

1 ? (3.4 x10^{13} p/cm^2/device x 5790 bits/device) = 5.07x10^{-18} cm^2/bit (2)

5.0 SOFT ERROR RATE PREDICTIONS

This section describes the derivation of the limiting SEU rates presented in section 1. They are calculated from the preceding limiting cross-section calculations to quantify the degree of proton SEU hardness demonstrated by the test. Consequently, these values are a representation of the test rigor rather than of any device proton SEU sensitivity. All SER calculations used the CREME96 code with solar minimum conditions and 100 to 150 mils Al shielding.

5.1 Extreme Worst-Case SER

The Extreme Worst-Case SER values of Table 1-I are calculated based on the following assumptions for both the flip-flop and configuration SRAM cells.

- ?? The SEU cross-section as a function of proton energy is defined by a Weibull distribution with the following parameters (E0, ?0, W, s).
  - ?? E0 = 45 MeV, per the HX6408 4M SRAM data of [5]
  - ?? ?0 is the 203 MeV limiting cross-section determined in this test and reported in section 4 for the optimized test orientation
  - ?? W and s parameters are 0.1 MeV and 1, respectively
- ?? The ?0 calculation considers only fluence accumulated at a 70° incidence angle. The SER calculation assumes the SEU cross-section is independent of proton incidence angle.

Table 4-I RHrFPGA Single Event Effects Test Log.

Part Number:	22024887-005	Test Facility:	Indiana University Cyclotron Facility (IUCF)
Manufacturer:	Honeywell	Ions:	Protons, 203 MeV
Description:	RHrFPGA, Digital ASIC, 0.35 micron, Custom	Test Date:	October 30, 2003
Device Serial nos:	1016-01, 1009-01, 1014-01 (date code 0314)	Test Personnel:	S. Buchner, H. Kim, T. Sanders (NASA), C. Ross, B. Burns, J. Lintz (Honeywell)
# Bits Tested:	Configuration: 131Kbits; Application: 5790 bits	Test Conditions:	3.0V supply, 25°C temperature, die cavity lids were not removed (~10 mil kovar)

Run #	DUT Serial #	Func-tional Test #	Test Name (Vector File)	Clock Freq. (MHz)	Angle (°)	Test Orien-tation	Proton Energy (MeV)	Run Fluence (#/cm2)	Run Time (sec)	Accum. Fluence (#/cm2)	Accum Dose (Krad(Si))	# Logic SEU	# Config SEU	Isupply DUT/CTRL (mA)	Comments
1	1016-01	1.0	Application	10	70	RAM	203	1.70E+12	88.1	1.70E+12	1.00E+02	0	0	129 / 250	Computer in test cell locked up. Not able to read config. RAM. Moved computer to better-shielded location.
2	1016-01	1.0	Application	10	70	RAM	203	1.71E+12	103.0	3.41E+12	2.01E+02	0	0	129 / 250	
3	1016-01	1.0	Application	10	70	RAM	203	3.40E+12	170.4	6.81E+12	4.01E+02	0	0	157 / 240	
4	1016-01	3.2	SR-Vert	10	70	RAM	203	3.41E+12	220.0	1.02E+13	6.01E+02	0	0	157 / 240	
5	1016-01	3.2	SR-Vert	10	70	RAM	203	3.40E+12	187.9	1.36E+13	8.01E+02	0	0	211 / 240	Is readings are for LBUS test
6	1016-01	3.6	SR-Lbus	10	70	RAM	203	6.81E+12	388.5	2.04E+13	1.20E+03	0	0	211 / 240	
7	1016-01	3.4	SR-Logic	10	70	RAM	203	6.80E+12	319.0	2.72E+13	1.60E+03	0	0	167 / 240	prerad Is = 167 and 240 mA.
8	1016-01	3.5	SR-Xbus	10	70	RAM	203	6.80E+12	335.7	3.40E+13	2.00E+03	0	0	155 / 240	156 and 240 mA prerad
9	1009-01	1.0	Application	10	70	RAM	203	6.82E+12	413.0	6.82E+12	4.01E+02	0	0	129 / 250	Is values were same pre-rad
10	1009-01	3.2	SR-Vert	10	70	RAM	203	6.81E+12	368.3	1.36E+13	8.01E+02	0	0	129 / 250	
11	1009-01	3.6	SR-Lbus	10	70	RAM	203	6.81E+12	341.3	2.04E+13	1.20E+03	0	0	211 / 240	Is values were same pre-rad
12	1009-01	3.4	SR-Logic	10	70	RAM	203	6.82E+12	373.4	2.73E+13	1.60E+03	0	0	166 / 240	166 and 240 mA prerad
13	1009-01	3.5	SR-Xbus	10	70	RAM	203	6.80E+12	371.1	3.41E+13	2.00E+03	0	0	155 / 240	
14	1014-01	3.8	5760	1	70	Flip-Flop	203	6.81E+12	406.6	6.81E+12	4.01E+02	0	0	30 / 118	31 and 118 mA prerad
15	1014-01	3.8	5760	1	70	Flip-Flop	203	6.81E+12	343.1	1.36E+13	8.01E+02	0	0	30 / 118	
16	1014-01	3.8	5760	1	70	Flip-Flop	203	6.81E+12	318.9	2.04E+13	1.20E+03	0	0	30 / 118	
17	1014-01	3.8	5760	1	70	Flip-Flop	203	1.36E+13	749.3	3.40E+13	2.00E+03	0	0	29 / 118	

Legend

Functional Test Number - Identifies the functional FPGA configuration tested and vector set. Corresponds to test documentation package.

Test Name - Name of test vector file used to evaluate the device under test, usually related to a specific functional block within the device.

Supply Voltage - supply voltage to the device under test, measured at the test device or test board.

Angle - Ion impingement angle on the DUT relative to the die's surface normal (a zero degree angle is perpendicular to the die surface).

Energy - Proton energy at the DUT, not corrected for minimal loss through package lid.

Test Orientation – Two orthogonal exposure angles were used, both maintaining a 70 incidence angle relative to normal incidence. One orientation “RAM” is worst-case upset in the configuration RAM cell; the other “Flip-Flop” is worst-case for upset in the application logic flip-flops.

Run Fluence - exposure run proton fluence in protons/cm2.

Accum. Fluence – cumulative proton fluence to which the identified device was tested.

Accum. Dose - total ionizing dose accumulated by the part under test.

logic SEU - number of single event upsets that occurred in the application during the exposure run

Config SEU - number of single event upsets that occurred in the Configuration SRAM during the exposure run

Isupply DUT/CTRL – post-exposure supply currents to the device under test (DUT) and controller chip (CTRL).

5.2 Nominal Upper Bound SER

The Nominal Upper Bound SER calculations use the following assumptions, which are less conservative that those of section 5.1.

- The SEU cross-section as a function of proton energy for both cell types is defined by a Weibull distribution with the following parameters (E0, ?0, W, s)
  - E0, W, s = 45 MeV, 15 MeV, and 1.0 per the HX6408 4M SRAM data of [5]
  - Weibull parameter ?0 is derived from the 203 MeV limiting cross-section for the optimized test orientation, with the following considerations
    - Variation of ?0 with incidence angle relative to the most sensitive path direction is equal to the HX6408 relationship from Figure 1 of [3].
    - A 90° angle is parallel to a cell's sensitive inter-transistor path, and 0° represents either normal incidence or an orthogonal grazing angle.

Figure 5.2-1 depicts the angular sensitivity data of [3], with the following function fit to the data. It approximates the cross-section as a function of incidence angle relative to the sensitive ion path direction, where 90° is parallel to the path and 0° is perpendicular.

$$?(?) = ?(0°) \times e^{(2.24(\sin(?))^{1.32})} \quad (3)$$

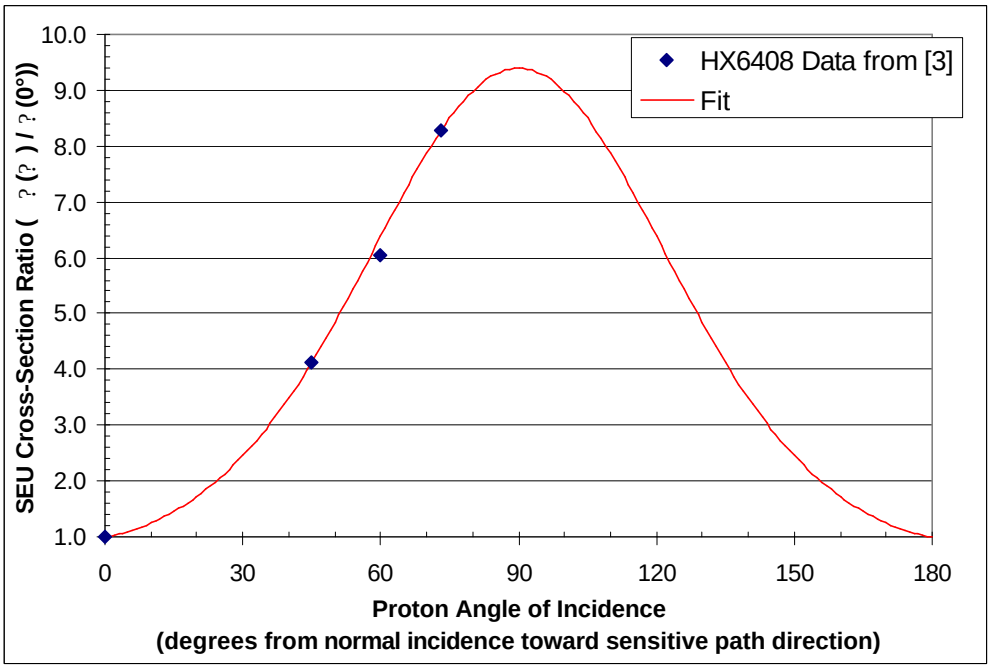


Figure 5.2-1 Approximation of SEU Cross-Section Angular Sensitivity.

Based on the HX6408 data, the SEU cross-sections for both RHrFPGA cell types at 70° are approximated as 7.87 times the values at normal incidence (0°). Thus, the 70° limiting cross-sections are re-calculated to include 12.7% of the exposure fluence at normal incidence, and the limiting cross-sections at 0° are calculated to be 12.7% of the new 70° values. The estimated RAM and flip-flop cross-sections at 0° are therefore

$1.34x10^{-20}$ cm^2/bit and $5.14x10^{-19}$ cm^2/bit, respectively.

For these calculations, proton SER for a given orbit and shield thickness is a constant multiple of the proton limiting SEU cross-section. The limiting SER values of Table 1-1 are readily calculated by integrating (3) over a 4-pi steradian solid angle. It is important to note the reverse angle of incidence convention used in Figure 5.2-1 and (3) and to note that angular symmetry applies to the sensitive heavy ion path between two transistors in a cell instead of to a vector normal to the die surface.

6.0 NOTES

6.1 Acronyms

Acronym	Definition
FPGA	Field Programmable Gate Array
GSFC	Goddard Space Flight Center
IC	Integrated Circuit
IUCF	Indiana University Cyclotron Facility
RAM	Random Access Memory
RERP	Radiation Effects Research Program
RHrFPGA	Radiation Hardened reprogrammable Field Programmable Gate Array
SEE	Single Event Effects
SET	Single Event Transient
SEU	Single Event Upset
SER	Soft Error Rate
SRAM	Static Random Access Memory

6.2 References

[1] – Sawyer, D. M. and J. I. Vette, “AP-8 Trapped Proton Environment for Solar Maximum and Solar Minimum”, Report NSSDC/WDC-A-R&S 76-06, Greenbelt MD, 1976.

[2] – A.J. Tylka, et al, “CREME96: A Revision of the Cosmic Ray Effects on Micro-Electronics Code”, *IEEE Trans. Nucl. Sci.*, 44, 2150 (1997).

[3] – R. A. Reed et al., “Evidence for Angular Effects in Proton-induced Single Event Upsets”, *IEEE Trans. Nucl. Sci.*, Vol. 49, pp. 3038-3044, Dec., 2002.

[4] – H. Y. Liu, K.W. Golke, D.K. Nelson, W. W. Heikkila, S.T. Liu, and W.C. Jenkins, “Proton Induced Single Event Upset In A 4M SOI SRAM,” presented at the 2003 IEEE SOI Conference, Newport Beach, CA.

[5] - S. T. Liu et al, “Single Event Effects in PDSOI 4M SRAM Fabricated in UNIBOND”, *IEEE Trans. Nucl. Sci.*, in press, (2003).

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